REMARKS

A Petition (and fee) for a three-month Extension of Time and an Excess Claims Fee letter and fee are filed concurrently hereto.

It is noted that the claim amendments herein are intended solely to more particularly point out the present invention for the Examiner, and not for distinguishing over the prior art or the statutory requirements directed to patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 2, 3, 10-12, 18, and 19 are all of the claims currently pending in the Application. Claims 13-17 are canceled above. New claims 18 and 19 are added. Claims 2, 3, and 10-17 stand rejected under 35 USC §102(b) as anticipated by Applicant's Admitted Prior Art (AAPA). Claims 2, 3, and 10-17 stand rejected under 35 USC §102(e) as anticipated by Kim.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed in, for example, claim 2, the present invention is directed to an input circuit that includes a data input means for receiving input data of the input circuit. A data latch means latches output data of the input circuit. A reset means resets the data latch means in response to a first logic level of a first clock signal.

A latch enhancement means enhances a latching operation of the data latch means in response to a first logic level of a second clock signal that is delayed in phase from the first clock signal. A clock synchronization means transfers the input data from the input means to the data latch means in response to a second logic level of the first clock signal, the clock synchronization means blocking a feedthrough current that flows through the reset means, the data latch means, and the latch enhancement means when the first and second clock signals are in a first logic level state.

Compared to the prior art discussed in Figure 6, the present invention, by blocking feedthrough current, reduces the power consumption of the device by eliminating the feedthrough current paths during data resets.

II. THE 35 USC §112, SECOND PARAGRAPH, REJECTIONS

All claims stand rejected under 35 U.S.C. §112, second paragraph, as being "indefinite". Applicant believes that the above claim amendments appropriately address the Examiner's concerns for antecedent bases.

Given the above clarifications, Applicant respectfully requests that the Examiner reconsider and withdraw these rejections.

III. THE PRIOR ART REJECTIONS

The Examiner asserts that AAPA anticipates claims 2, 3, 10, 12, 15, and 17. The Examiner alleges that transistor 9 serves the role as blocking feedthrough current.

Applicant respectfully disagrees.

As explained at lines 4-11 of page 9 and, more particularly, lines 5-15 of page 10 and contrary to the Examiner's allegation, this circuit does indeed have a feedthrough current problem as CK1 changes from high to low at time t = 2 and the clock signal CK2 changes from high to low at time t = 2'. Therefore, it is submitted that AAPA fails to show the means taught by the present invention to block this feedthrough current problem.

Hence, turning to the clear language of the claims, there is no teaching or suggestion in AAPA of " ...the clock synchronization means blocking a feedthrough current that flows through the reset means, the data latch means, and the latch enhancement means when the first and second clock signals are in a first logic level state ....", as required by claim 2.

Relative to claim 3, AAPA fails to teach or suggest: "... wherein said activating means blocks feedthrough current that flows through the reset means, the data latch means, and the latch enhancement means when the first clock signal is in a second logic level state and the second clock signal is in a first logic level state....."

Relative to the rejection based on Kim, Applicant first submits that this reference actually fails to qualify as prior art, since its US filing date of August 22, 2001, is later than the Japanese priority date of March 26, 2001, for the present Application. Thus, Applicant reserves the opportunity to file a verified translation of the priority document.

However, even if considered as prior art against the present invention, Applicant submits that the evaluation of record fails to heed the plain meaning of the claim language. The Examiner attempts to consider the terminology "blocking feedthrough current" as

referring to any circuit component that serves to prevent current from passing through that circuit.

Applicant submits that, having read the description at lines 5-15 of page 10, one of ordinary skill in the art would disagree with the Examiner's interpretation, since the term "feedthrough current" is clearly defined as the current that feeds through a series of transistors during a timing transition period.

The Examiner fails to identify any feedthrough current paths in Kim.

Therefore, absent such feedthrough current path, there clearly is no component in Kim that satisfies the description of blocking the feedthrough current path.

Stated slightly differently, Kim fails to have the two clocks CK1, CK2 shown in AAPA, let alone the feedthrough current path wherein current passes through transistors 3, 6, and 11.

For this reason, Applicant submits that the clocked enabling gates NB, ND of Figure 8 or the clocked enabling gates N0,N2 of Figure 10 fail to qualify as components that can reasonably be described as blocking a feedthrough current, as that term is defined in the AAPA.

In the present invention, latching operation of input data starts by the first clock signal (CK1) and the latch enhancement means starts by the delayed second clock signal (CK2)

In contrast, in Kim, the latching operation of input data and the latch enhancement means start by the same clock signal (CLK). Therefore, the drivability of transistors NB,ND must be larger than the drivability of transistors N0,N2, for latching operation. Accordingly, the input circuit of Kim suffers an inherent design difference in that it consumes more power than the input circuit of the present invention.

However, in a good faith attempt to expedite prosecution, Applicant has amended the independent claims to define the specific feedthrough current that is blocked by the present invention.

Hence, Applicant submits that Kim fails to teach the same claim limitations as identified above for AAPA.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with the AAPA or Kim, fails to teach or suggest the claimed invention.

IV. FORMAL MATTERS AND CONCLUSION

The Examiner objects to the specification because of the Abstract and the typographical error in the final line of page 12. Applicant submits that the revisions above address the Examiner's concerns and request that the Examiner reconsider and withdraw these objections.

In view of the foregoing, Applicant submits that claims 2, 3, 10-12, 18, and 19, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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